Plans to post fab 8 made in 2004

In 2004 I did a self evaluation on my skills.

I At the time had experience In testing at the Level of Wafer Level The problem is that this is linked to a old platform Trillium

I was of the impression that my career development was a partnership between me And my employer.
I told my managers at Fab 8 that I planned to change My path after the end of the legacy products.

Vision of Intel Fab8 in 2004

The Fab made plans to convert to a memes fab in 2007.That meant the end of my Job at wafer sort.

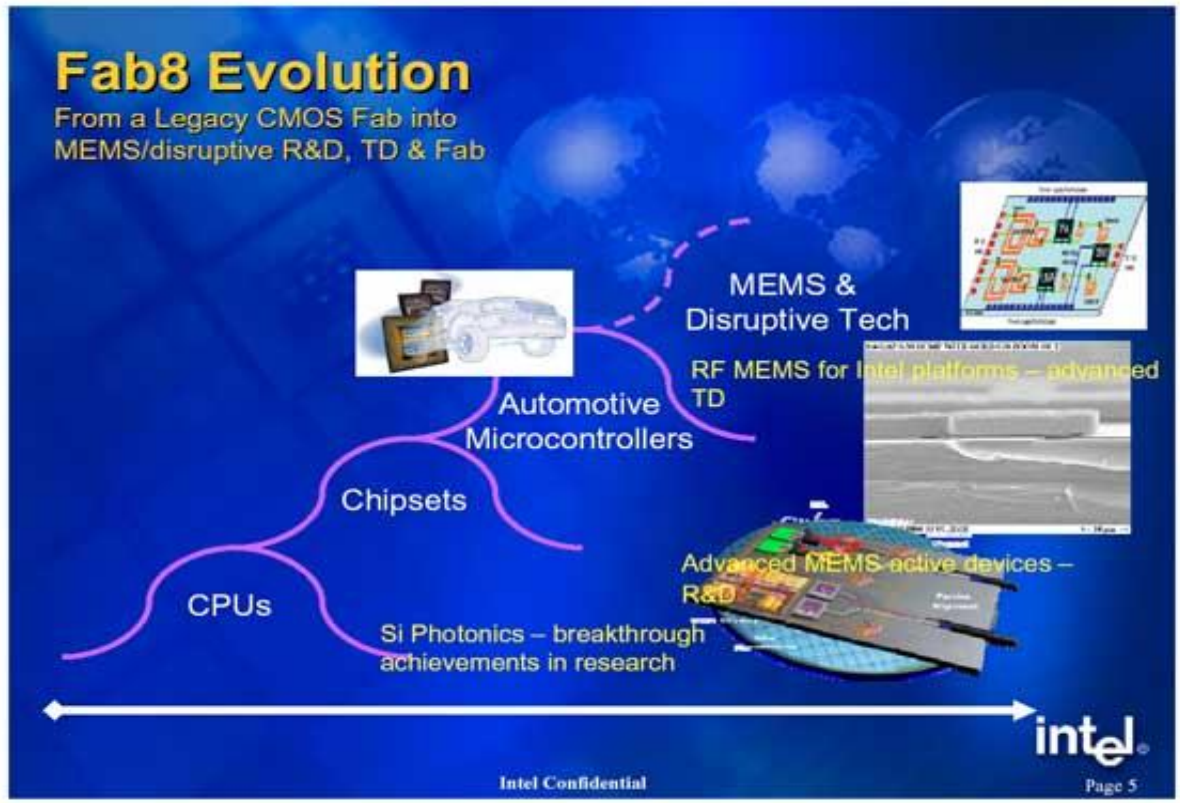
The Idea was to build RF filters for Wifi at the fab post 2007.
I did not see Intel serious about this plan outside of fab 8.

What added value is there for Intel to make RF filters when Coilcraft are experts at making filters?

As I predicted the mems Idea was scrapped in 2005 months before fab 28 was announced

Fab 8 vision 2004

http://ixbtlabs.com/articles2/cm/intel-israel-dec2



What Fab 8 planned to do after 2008

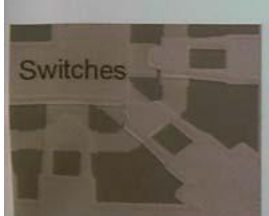
Surface Micromachining

- Definition: MEMS that are made using films deposited on a wafer
  - The structural layer has the desired mechanical, electrical, and thermal properties, etc.
  - The sacrificial layer supports the structural layer until it is etched – the "release etch"

Intel's MEMS Capabilities

- Surface and Bulk micromachining technologies
- Advanced Packaging research

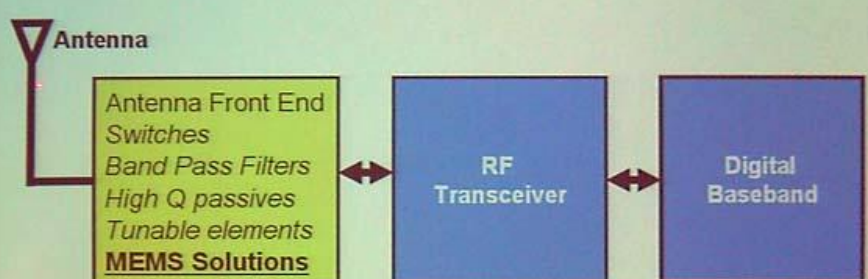
Examples of experimental RF components fabricated at Intel



Packaged MEMS devices

Slide 11

Wireless system block diagram



- MEMS components switch, filter and condition the antenna signals prior to the RF transceiver
- MEMS Value Proposition
  - Lower insertion loss
  - All Silicon based
  - Smaller form factor with silicon integration
  - Addresses the RF complexity of current and future multi standard radio coexistence

Slide 8

Moving from Wafer Sort to Validation

I started out looking to translate my skills in Wafer Sort Programs to Validation
Only Later to find different Validation is Validation checks a design for bug Wafer Sort test the manufacturing and Functionality they do overlap but not as much as I fist envisaged.

My starting point was VHDL

I took a course private at Hi-tech

November 2004

In the middle of November 2004 IDC Haifa were looking for people to work At HVT and SV (Silicon Verification).
It Took HR at IDC until The Middle of March 2005 to get back to me that they did not want to interview me.(No Reason given)

The Job At SV open in Jobs Online till May 2005.
This may be due to the bad Annual review of 2004.

In 2005

I took the second course and invested in the Spartan3 Xilinx kit and did the Advanced VHDL course

In the second half of 2005

I created a VHDL design a chip that had A built in
VGA driver (640*480) 25 lines Text 80 colums
PS2 keyboard
Stepper Motor driver (Half step)
RGB Led driver (PWM 4096 colors)

I wanted to create a 6502up using Verilog and
Join it to the existing design in VHDL

Problems

I did not understand the complexity of mixing VHDL with Verilog as the Free Version of Modelsim did not support simulation of mixed languages.
My only support was Xilinx and some user groups I got no support at all internal within Intel

In November 2005

I shelved the 6502 I had taken for granted that Intel was going to be

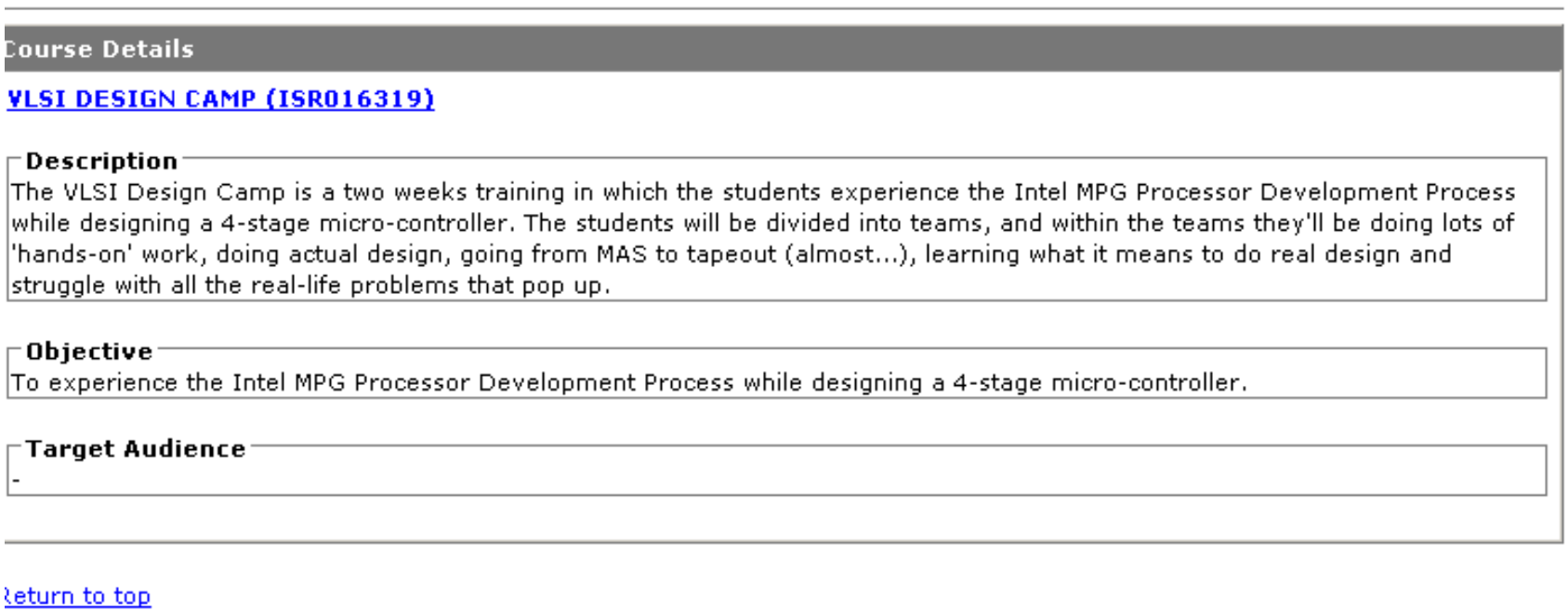
suportive in gaining skills like VHDL Verilog and System Verilog

http://www.6502.org/
Here is an Idea of the project Size I wanted to create
http://www.opencores.com/projects.cgi/web/system09/overview

Intel Course

- This is the Intel Internal course that I needed to do so as to get the
- skills to start a full micro processer design.

Note a internal course almost no cost to Intel not a vendor course.But outside of the Fab.Intel saw no added value in helping me



Course Details

VLSI DESIGN CAMP (ISR016319)

Description

The VLSI Design Camp is a two weeks training in which the students experience the Intel MPG Processor Development Process while designing a 4-stage micro-controller. The students will be divided into teams, and within the teams they'll be doing lots of 'hands-on' work, doing actual design, going from MAS to tapeout (almost...), learning what it means to do real design and struggle with all the real-life problems that pop up.

Objective

To experience the Intel MPG Processor Development Process while designing a 4-stage micro-controller.

Target Audience

-

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Feb 2006

I in 2006 went on to start learning Verilog once again private no help from Intel

סלע יוניברסיטי וסיטל טכנולוגיות
מתכבדים להעניק בזאת

תעודת סיום

לכבוד

אריה לשנסקי

בעבור השתתפות בקורס

תכנון ב Verilog לפיתוח חומרה

בהיקף 27 שעות
אשר התקיים בסלע יוניברסיטי והסתיים
ביום 8 לפברואר 2006

SITAL Technology

SELA university

Nov 2006

I did a course also only three days in System Verilog once again Not the Intel U. Again the Intel U course was a internal course no real cost to Intel.

Jerusalem

Course Details

SYSTEM VERILOG VERIFICATION (PDT028815)

Description

This 3 day course is aimed at experienced Verification engineers who wish to learn about the exciting verification features of SystemVerilog. The course stresses a methodology for implementing these features in your verification environment. This course is taught for all the leading simulators although not all simulators will support every feature immediately. The course is a consistent mix of lecture and lab-exercises. Targeted quizzes and labs are designed to reinforce the course material. Some of this class overlaps our SystemVerilog for Designers course.

Objective

Course Outline SystemVerilog Datatypes Arrays & Structures Tasks & Functions Hierarchy SV for Verification Transaction based Verification Methods & process control Hierarchy Program Blocks (PB) Clocking Domains Interfaces Simple bundle Methods & Modports Transactors & Monitors Lab SV Classes OOP (Object Oriented Programming) Copying, Inheritance Constructors Virtual methods Scoreboarding Lab Randomization & Constraints Stimulus Methodologies Random Testing Directed Random Testing rand, randc type modifiers Constraint Block Overloading, Iteration Dynamic Constraint Changes in SV randomize() Non-OO randomization Random/Constraint control randcase / randsequence / weighting Lab Functional Coverage Coverage Driven Verification (CDV) Why do CDV? Coverage (Structural vs Functional) Covergroup / coverpoint / cross Coverage sampling Options and type_options Lab SVA SystemVerilog Assertions Repetition & other operators Sequences / properties / directives Reactive SV testbenches Lab

The Issue

Intel did not to give any support In gaining skills that I need even when the writing was on the wall.
The Courses I needed were all Internal “NOT VENDOR” and a very low cost to the company.

With a Design Center just Meters away I need to go to internet user groups for support was a disgrace.

Intel has high walls between “Design" and “Fabs" I needed support from design but was part of a Fab

To Quote production manager in a “Open Forum “Meeting

“Intel Fab8 will not open any doors that the employee can not open by himself If he was of the opinion that he had what it takes why did I not apply and let his skills speak for him”
Here Is my Reply

.In 2006 I was declared to be a Anchor in the Fab that means I can not apply for Internal Jobs !!
.In 2007 I was part of the closure Team of Fab 8
If I wil have declined being part of the closure team I will have lost 20% of my severance package

Here to no option to apply for Internal Jobs till the end of
I needed support in 2004 to 2008 to gain skills but the d the Fab

If I will have declined the Closure team

I will not have got even less support if possible.
As the Fab will not help a person jump ship that It needs until it is ready to kick him out.
I will have just lost the closure bonus.

So in 2006 and Most of 2007 Intel Effectively closed Doors

Final Words

I am not attempting to attack my past employer but to show the process I started in 2004

I was wrong to take for granted that my employer will see my gaining skills in VLSI design and validation not as a “Win & Win “

This may help some employee at Intel who thinks that Intel is a place that you will get support. I tried three years and got no support